# First Experimental Demonstration of Dual-sided N/P FETs in Filp FET (FFET) on 300 mm Wafers for Stacked Transistor Technology in Sub-1nm Nodes

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## Abstract

For the first time, dual-sided devices in Flip FET (FEET) were successfully demonstrated on 300 mm wafers, on which the FFET's unique back-to-back stacking of frontside (FS) NFET and backside (BS) PFET were realized. A series of key process modules including wafer bonding, substrate thinning, channel profile optimization, litho overlay correction and BS performance tuning were successfully developed. As a result, FS NFET after flipping behaved well and decent BS PFET ($L_G$ of 30 nm, SS of 73.1 mV/dec, DIBL of 24 mV and on-off ratio of $10^7$) was achieved, comparable to the FS NFET. Thanks to the separated processes on each side of the wafer, this work further validates the outstanding features of FFET: natural split-gate, good multi-$V_t$ tunablity (~ 500 mV) and better process margin without challenging high aspect ratio vertical patterning as required by CFET. Moreover, dual-sided CMOS was also realized, proving the excellent extendibility of FFET. With the great benefits in process-friendliness, design flexibility and scalability as compared with CFET, FFET is validated to be a crucial candidate for logic nodes beyond 1nm.

## Introduction

As the transistor scaling approaches its physical limit, novel architectures play critical roles in technology development (see Fig. 1). Advanced device structures such as Gate-All-Around (GAA) Nanosheet (NS) [1-3], Forksheet [4], vertical GAA [5-6] and the Complementary FET (CFET) [7-13] are widely discussed. In parallel, the wafer backside interconnects for power, clock and signal [9-11, 14-16] are also on the roadmap. By seamlessly combining both, the FFET [17] stacks transistors and interconnects in a symmetrical back-to-back fashion with self-aligned (SA) active and dual-sided power / signals, fully exploiting potentials of both sides of the wafer with much relaxed process requirement (aspect ratio, split-gate and multi-$V_t$) and enhanced design flexibility and routability.

For here, we demonstrated dual-sided N/P FETs in FFET on 300 mm wafers, with key processes developed. The frontside (FS) FETs before & after flip (FS FETs & flipped FS FETs) and backside (BS) FETs are carefully characterized. Other crucial advantages of FFET, such as dual-sided CMOS, simpler $V_t$ tunability, natural split-gate are also discussed. In the end, FFET is benchmarked with other stacked transistor technologies.

## Process Development

Fig. 2 shows the key steps of FFET process flow. The FS and BS fin actives were formed in a self-aligned manner, followed by splitting the FFETs into FS FETs, flipped FS FETs and BS FETs to investigate the impact of FS and BS processes. There are three critical process modules for FFET other than standard FS FinFET processes:

***A. Wafer Bonding and Thinning:*** After the edge trimming (Fig. 3(a)), the device wafer was bonded to a carrier wafer with strong bonding strength and clean interface (Fig. 3(b)). After flipping, grinding was firstly used to remove most of the substrate Si, followed by a highly selective wet etch (SiGe/Si selectivity ~ 200) stopping on the SiGe etch stop layer (ESL) as in Fig. 2(e). Then, the ESL was selectively removed from Si. This series of selective etching ensures good control of the total thickness variation (TTV). The remaining Si was finally removed by a CMP stopping on STI, demonstrated by the precise stop position and surface flatness in Fig. 3(f).

***B. Backside Channel Profile Optimization:*** Inherited from the FS fin etch, the backside active fin has an undesired and reverse-tapered profile, as shown in Fig. 4(a). To solve this issue, BS fin trimming based on ion beam etch (IBE) was first explored (Fig. 4(b)), which provides a tapered BS fin profile but some ion bombardment damages. A novel method (Fig. 4(c)) was also developed, delivering nearly straight fin profiles for both FS and BS with intact Si crystal structure. The TCAD simulations in Figs. 4(d-e) further validate the benefits of the optimal fin profile by novel method for both gate control and channel strain.

***C. Backside Lithography Overlay Correction:*** Fig. 5(a) shows the worsened BS lithography overlay due to the wafer distortion coming from bonding and substrate thinning. A new correction model was applied (Fig. 5(c)), reducing the BS overlay residue by >70% with tighter distribution (3σ value ~4.4 nm), as in Figs. 5(b, c).

By combining these crucial modules of FFET with standard FinFET processes, both flipped FS FETs and BS FETs in FFET were realized (Fig. 6). The dual-sided FETs feature $L_G$ of 30 nm and almost symmetric device geometry and interconnects.

## Electrical Characteristics

The fabricated BS PFETs and flipped FS NFETs were both measured from the backside, as in the inset of Fig. 7. Fig. 7(a) shows the $I_D$-$V_G$ curves of the BS PFET and the flipped FS NFET. The $I_D$-$V_D$ curves in Fig. 7 (b) further validate nearly symmetric on-state performance, which is crucial for CMOS.

***A. BS PFET Performance Improvement:*** Fig. 8(a) illustrates the $I_D$-$V_G$ curves of the unoptimized and optimized BS PFET for 30/240 nm $L_G$ devices. The current drivability and gate electrostatics (Figs. 8(b-c)) were greatly enhanced by contact optimization and EOT thinning (condition #1 to #2). By further tunning the junction proximity, gate work function and interface trap density ($D_{it}$), 137% higher on-state current, $SS_{Lin}$ of 73.1 mV/dec and DIBL of 24 mV were realized, which are comparable to the flipped FS NFET (not shown).

***B. FS NFET with BS Thermal Processes:*** BS Thermal budget impacts were studied by annealing the FS NFET (Fig. 9). The thermal budget is divided into bonding thermals (1st anneal) and BS device fabrication thermals (2nd anneal), as shown in Fig. 9(a). It shows minor changes for bonding thermals but clear impacts from BS device fabrication processes, indicated by the $V_t$ shift, smaller current and degraded gate electrostatic (Fig. 9(b)). More serious studies are needed. However, unlike the sequential(seq.) CFET with strict limits, multi-flipping strategy can be used for FFET [18] to relax the thermal budget issues, which provides a solution to complete the FS device's gate and BEOL processes after the BS device's processes.

***C. Dual-sided $V_t$ Tuning in FFET:*** Fig. 10(a) shows that dual-sided multi-$V_t$ process is simple and straightforward for FFET by applying the industry standard process on each side of the wafer for N/P FETs, as proven by the dual-sided $V_t$ tunability (~ 500 mV) in Fig. 10(b). However, for monolithic (mono.) CFET, it's technically hard due to the very complex vertical patterning (VP) process [10] with high AR. The VP process requires timed etch of gate stacks, which is difficult to steadily control the etch rate and etch residuals. The VP process also prevents CFET from easily making split gate structure, which is quite natural for FFET, as in Fig. 10(c). Moreover, the switch between split gate and common gate is smooth for FFET by the gate merge [17] process, endowing FFET with more flexible designs.

***D. Dual-sided CMOS by FFET:*** Thanks to the separated processes on each side as in Fig. 10(a), FFET can support coexistence of NFETs and PFETs for both FS and BS, enabling even more flexible and scalable designs than mono. CFET, such as bipolar SRAM [17]. The FFET's dual-sided CMOS characteristics are shown experimentally in Figs. 11(b, c), indicating matched performance for N/P FETs.

## Conclusion

For here, we experimentally demonstrated the symmetric dual-sided N/P FETs in FFET for the first time. The FFET outperforms CFET in the aspects of process difficulty, design flexibility and scalability, as summarized in Table. I, proving that FFET is a crucial candidate for future's 3D stacked transistor technology.

## Acknowledgement

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## References

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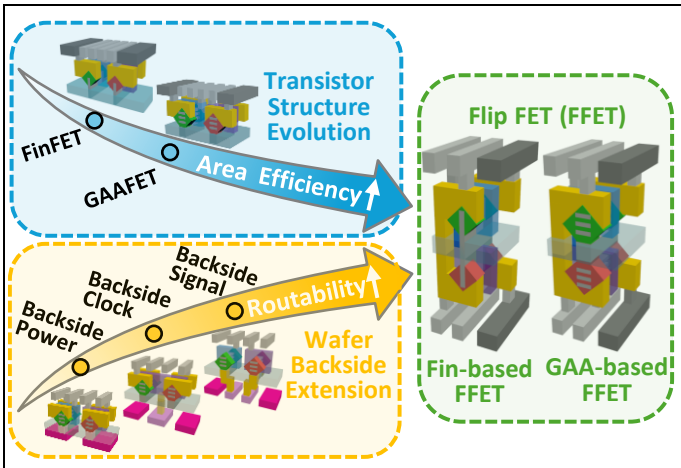



Fig. 1. Advanced logic technology roadmap with 3D transistor structures and backside interconnects, trending towards the Flip FET (FFET), a novel stacked transistor technology with symmetric dual-sided devices and interconnects. Combining the advantages of 3D transistor architecture and wafer backside interconnects, the FFET exhibits superior scalability and routability as the potential ultimate form of 3D stacked transistors.

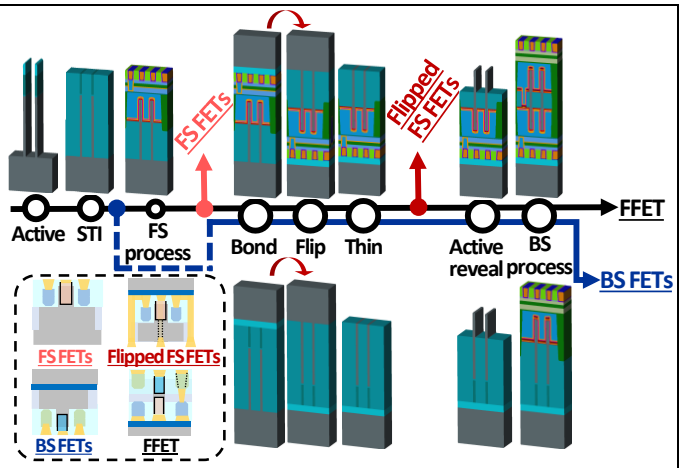



Fig. 2. Schematic process flow of FFET with dual-sided processes. Its N/P processes are decoupled, with standard aspect ratio as the FinFET. The complete FFET flow includes FS industry-standard process, wafer bonding, flipping, substrate thinning, active reveal and BS processes. BS FETs are formed by skipping some FS processes. FS FETs are obtained with standard FinFET process, after which flipped FS FETs are obtained after bonding/flipping/thinning.

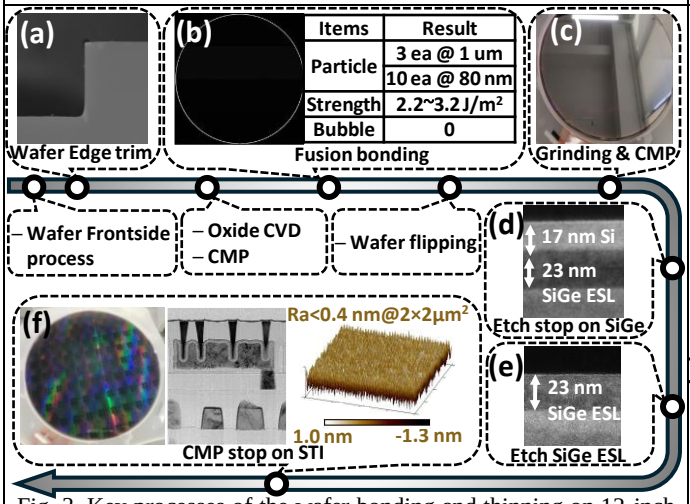



Fig. 3. Key processes of the wafer bonding and thinning on 12-inch wafers: (a) Wafer edge trimming. (b) Wafer fusion bonding readouts: The scanning acoustic microscope image (left) and bonding quality (right). (c) Wafer after grinding & CMP. (d) Substrate Si etch. (e) Substrate Si removal stop on SiGe ESL. (f) Si CMP stopping on STI bottom: wafer (left), TEM image (center), AFM result (right).

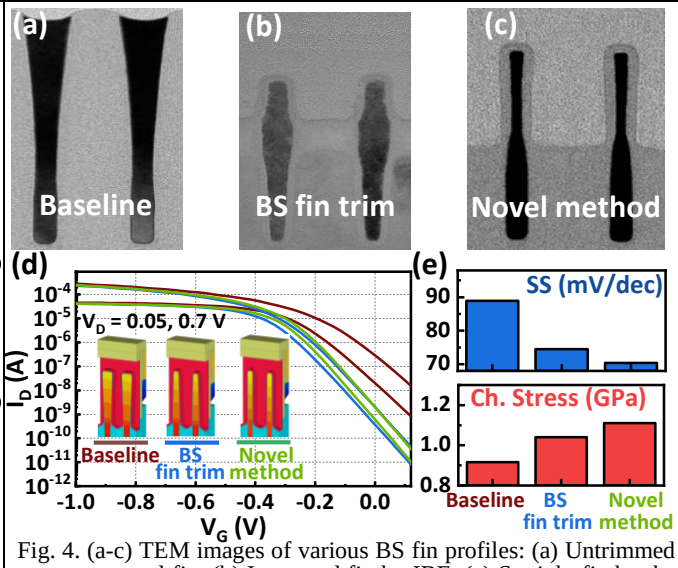



Fig. 4. (a-c) TEM images of various BS fin profiles: (a) Untrimmed reverse tapered fin. (b) Improved fin by IBE. (c) Straight fin by the novel method. (d-e) TCAD simulation of PFETs with different BS fin profile: (d) transfer curves, (e) SS and channel stress.

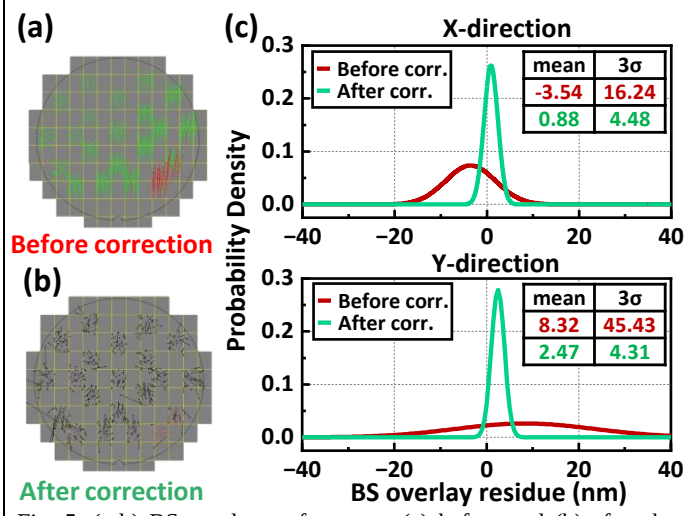



Fig. 5. (a-b) BS overlay wafer maps: (a) before and (b) after the correction. (c) Distribution of BS overlay residue before and after overlay correction in the X-direction (top) and Y-direction (bottom). With mean value < 3 nm and much tighter distribution, the overlay residue is well controlled after the correction.

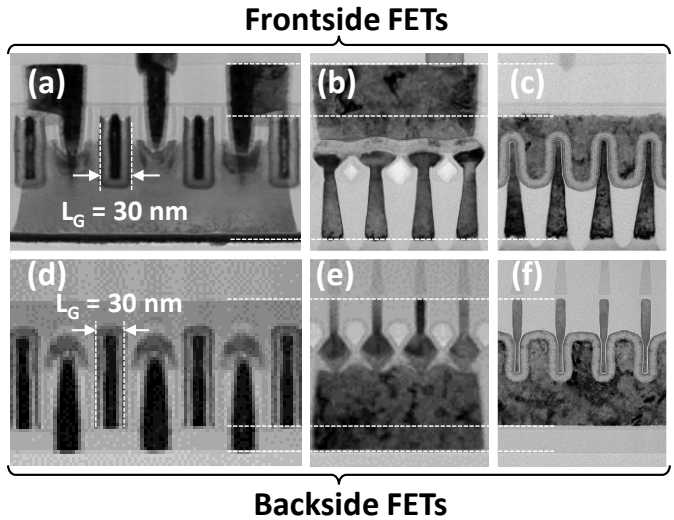



Fig. 6. TEM images of flipped frontside FETs: (a) cross gate, (b) cross fin on SD and (c) cross fin on gate after wafer bonding, flipping and substrate thinning. TEM images of backside FETs: (d) cross gate, (e) cross fin on SD and (f) cross fin on gate.

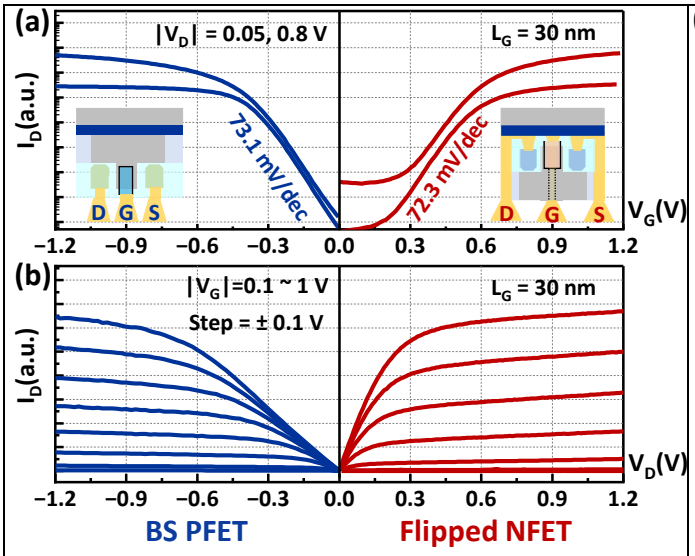



Fig. 7. (a) $I_D$-$V_G$ characteristics of BS PFET and flipped FS NFET at $|V_D|$ = 0.05, 0.8 V. (b) $I_D$-$V_D$ characteristics of the BS PFET and flipped FS NFET. The $I_D$ is normalized to effective gate width.

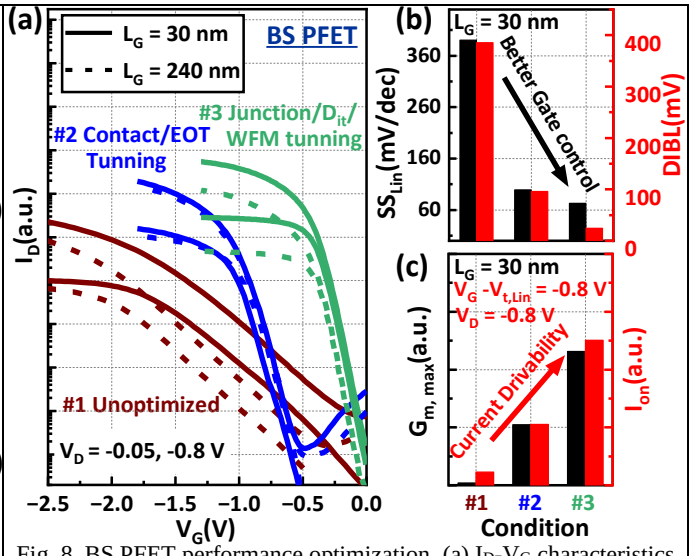



Fig. 8. BS PFET performance optimization. (a) $I_D$-$V_G$ characteristics of unoptimized and optimized BS PFETs for both short and long channel devices. (b) Gate electrostatics improvement (SS, DIBL). (c) Current drivability enhancement ($G_m$, $I_{on}$).

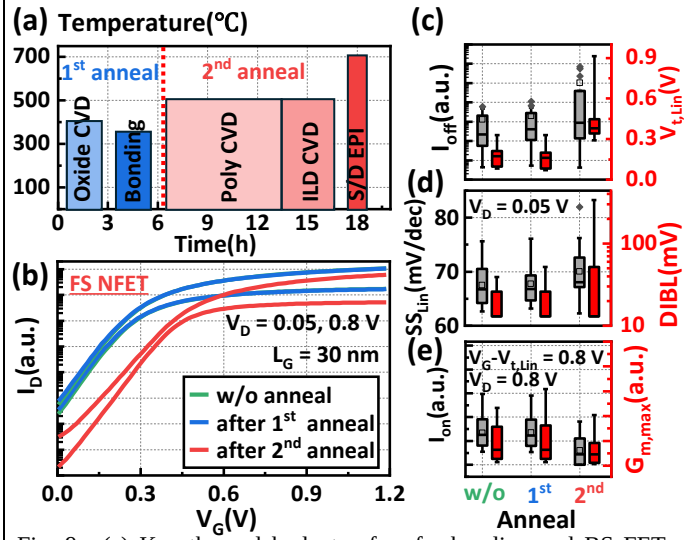



Fig. 9. (a) Key thermal budgets of wafer bonding and BS FETs processes. Annealing experiments are highlighted. (b) $I_D$-$V_G$ curves of FS NFET before and after annealing experiments. (c-e) Key device metrics before and after annealing experiments.

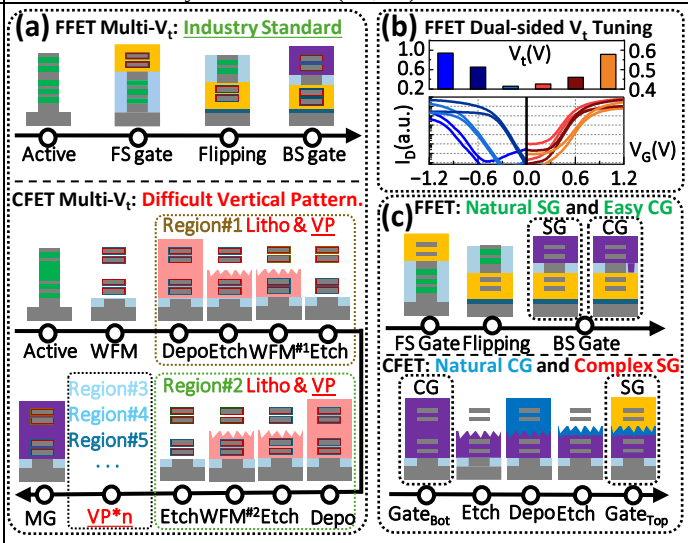



Fig. 10. (a) FFET multi-$V_t$ strategy with industry standard process and the complex multi-$V_t$ strategy for CFET, with vertical patterning. (b) Dual-sided $V_t$ tuning readouts in FFET. (c) SG and CG strategy of FFET and CFET. FFET features natural SG.

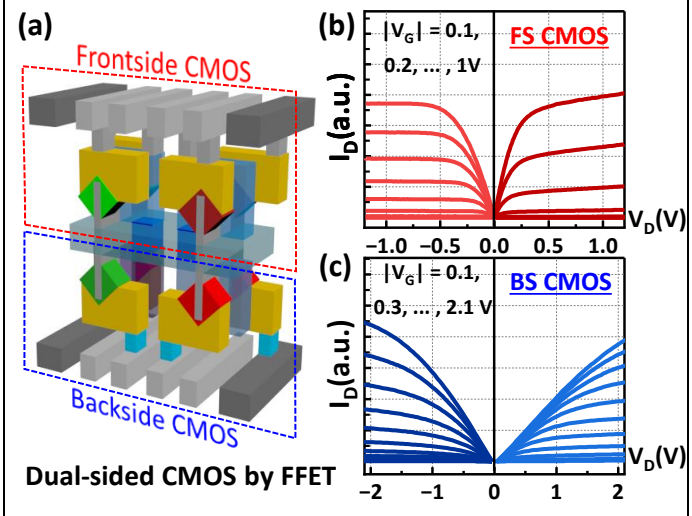
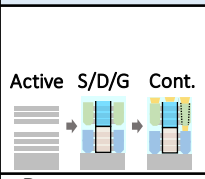
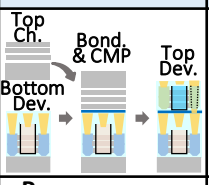
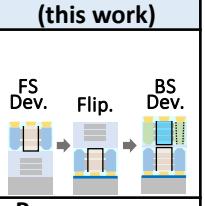



Fig. 11. (a) 3D schematic of dual-sided CMOS concept by FFET. Thanks to the separated FS/BS processes in FFET, dual-sided CMOS were successful demonstrated: (b) $I_D$-$V_D$ curves of flipped FS CMOS and (c) Preliminary $I_D$-$V_D$ curves of BS CMOS.

TABLE I. Benchmark of CFET and FFET based on Nanosheet

| | Mono. CFET[8-12] | Seq. CFET[13] | FFET (this work) |
|---|---|---|---|
| Process |   |   |   |
| Pros. & Cons. | • Process<br>• SA-active<br>• High-AR<br>• No thermal budget concerns<br>• Design flexibility<br>• No Multi-$V_t$ solution<br>• Unsolvable Split Gate<br>• Scalability<br>• Good (symmetric interconnects but asymmetric devices) | • Process<br>• Non SA-active<br>• Low-AR<br>• Serious thermal budget concerns<br>• Design flexibility<br>• Friendly Multi-$V_t$<br>• Natural Split Gate<br>• Scalability<br>• Bad (asymmetric interconnects and devices) | • Process<br>• SA-active<br>• Low-AR<br>• Thermal concerns solvable by Multi-Flipping<br>• Design flexibility<br>• Friendly Multi-$V_t$<br>• Natural Split Gate<br>• Scalability<br>• Best (symmetric interconnects and devices) |

Cont.->Contact, Dev.->Device, Ch.->channel