First Demonstration of Symmetric Dual-sided Vertical FET (DSVFET) for Energy Efficient Computing (EEC): From Processes and Devices to Circuits

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Abstract: For the first time, we proposed and demonstrated the symmetric dual-sided vertical FET (DSVFET) experimentally. The DSVFET not only inherits the low leakage, drive voltage and parasitic benefits from the standard VFET but also features unique dual-sided S/Ds with smaller footprint and better symmetry, perfectly suiting for the energy efficient computing. A series of new processes and DTCO methods were developed to study the device structure, performance and circuit design. DSVFET with aggressive contact gate pitch (CGP) of 50 nm and minimum L_g of 19 nm was realized. DSVFET was also validated with nearly symmetric behaviors (ΔC_{eff} & Δdelay < 3%) and 38%/60% lower power than FinFET for 2 nanosheets (2NS) and 1NS design at iso-frequency based on ring oscillator (RO) simulation respectively. A RISC-V core was used for block level evaluation and 17.4% lower energy, 15% lower energy delay product (EDP) and 39.8% smaller areas were identified for the 1NS DSVFET with PowerVia (PV). DSVFET has proved to be a great candidate for future's EEC.

Introduction: With the rapid advancing of AI, the energy wall is inevitably close, demanding greener solutions. Especially, edge AI requires even higher energy efficiency (EE) [1], More efficient computing paradigms are widely discussed beyond the conventional high performance computing (HPC) and general purpose computing (GPC) [2], urging deeper exploration into the EEC.

VFET is a much more suitable option than FinFET for EEC [3] (Fig. 1). It features the gate-all-around (GAA) channel with vertically placed S/D/G, providing less leakage, lower V_{DD} and smaller parasitic RC without area tradeoff [4]. More importantly, VFET has smaller footprint thanks to its vertical nature and the zero diffusion break (ZDB) [5], reducing the load capacitance and resistance. However, the asymmetric S/D stops it from practical use and the bottom electrode also wastes area [6]. For here, following the line of optimizing the device asymmetry, Frontside VFET (FSVET), Backside Contact VFET (BCVFET) and DSVFET are comprehensively benchmarked with FinFET in the aspects of the process development, device optimization, circuit and block design with DTCO methodology, validating the great advantages of the DSVFET proposed in this work.

Device Fabrication: Fig. 2 summarizes process flow of DSVFET. After forming the front epitaxy (epi) and contact, a carried wafer is bonded and flipped. The active wafer's substrate is thinned down by CMP stopping on the STI, which is then removed to reveal the vertical NS. In following, the gate process and back spacer formation are done. In the end, the back epi is grown directly on end of vertical NS to form the symmetric S/Ds of DSVFET, followed by contact formation.

Critical process modules were developed, including high aspect ratio vertical NS etch (Fig. 3(a)), gate stack deposition (Fig. 3 (b)), gate recess (Figs. 3(c-e)) and front epi growth (Fig. 3(f)). The integrated processes were also conducted step by step as shown in Fig. 4, delivering the world's first structure validation of DSVFET with aggressive CGP of 50 nm and L_g of 19 nm. It clearly demonstrates the symmetric S/D epi and contact with well-formed gate structure, proving the process feasibility of DSVFET.

Asymmetry and Performance Optimization: A Physical TCAD model of FSVFET was first established and calibrated to ref. [5], with matched structure and characteristics (Fig. 5(a)). It's then migrated to BCFET and DSVFET with design rules (shown later in Tables I-II) matched with advanced nodes. With the most symmetric structure (Fig. 5(b)), DSVFET has the best device symmetry. Its I_d-V_g (Fig. 5(c)) and C_{gd}/C_{gs}-V_g curves (Fig. 5(d)) in forward (FWD, front epi as drain) and reverse (REV, back epi as drain) modes almost coincide, showing minor C_{eff} differences of 2%/1% for N/P (Fig. 5(e)) and 2%/2% delay @ iso-I_{off} difference for N/P. Note that, the difference of C_{gd} at V_g of the three types of VFET is mainly due to changed channel capacitance caused by different fabrication processes.

Further performance optimization was also conducted. As shown in Fig. 6, DSVFET features unique freedom in tunning L_g and spacer thickness in the vertical direction, unleashed from the CGP constraint [3]. Increasing L_g gives lower leakage but worse delay due to larger channel capacitance. While, tradeoff can be seen in increasing the front/back spacer thicknesses considering that they have different effects on delay, resulted from the I_{eff} and C_{eff} changed simultaneously.

Novel Dual-sided Design and PPA Analysis: Considering the dual-sided structure and symmetric characteristics of DSVFET, backside local routing was introduced for better design flexibility without concerning the current flow direction. Note that dual-sided power is required. As in the AOI21 example from Fig. 7(a), V_{SS} needs to be placed at both the frontside and backside to avoid using super via (SV) of huge RC penalties, with frontside power rails connected to the backside by power tap cells [7]. Moreover, the NS number (1NS, 2NS) and NS placement orientation (xNS, yNS) of DSVFET were also studied, as in Fig. 7(b). Besides, for key sequential logics with transmission gate (TG), common gate (CG, Fig. 7(c)) and split gate (SG, Fig. 7(d)) should also be considered [8].

Uniquely, as highlighted in Fig. 8 for the MUX2D1 cell, DSVFET can support new logic cell designs using the CG design by abutting transistors with same input signals (e.g. N/P FETs in different TGs but with same clock signals) without area penalty and extra routing resources, thanks to it's dual-sided routing and independent S/Ds to other devices. For fair comparison, 2NS DSVFET and 1Fin FinFET were used due to their similar W_{eff}, with design rules listed in Table 1, considering the minimum space and gear ratio between metal layers.

A 15-stage FO3 RO with distributed BEOL load extracted from STA and P&R critical path statistics of a RISC-V core was used for the evaluation [9], at V_{DD} = 0.35 V according to [2]. Power @ iso-frequency of 2xNS-CG is 39%/16.2% less than FinFET without/with BEOL load, respectively. It's reduced more by 38% on 2yNS-CG with BEOL load due to its smaller cell area in the y direction (Fig. 9(a)). Furthermore, the pin placements on M0 and the shape of the M0 were also studied on larger cells such as INVD2 (Fig. 9(b)) and INVD8 (Fig. 9(c)), delivering further 6% and 20% higher frequency @ iso-power respectively due to smaller parasitic RC.

Ultimate Block-level Scalability: DSVFET can be further scaled with 1NS design. Based on PPA results of 2NS above, 1xNS and 1yNS with CG design and PowerVia were studied as in Fig. 10(a). For the PV, it was only inserted in 1xNS due to area penalty in 1yNS. In the form of a trench filled with metal, PV can replace power tap cells [10], saving extra area at the block level. It also helps eliminate the frontside power rail, relaxing the M0 pitch (Table 2). 1NS DSVFET cell areas are smaller than FinFET (Fig. 10(b)). The circuit level PPA (Fig. 11(a)) further indicates 41% lower power @ iso-frequency than FinFET for 1xNS (W/O BEOL load) and 60% for 1xNS-PV (W BEOL load).

The block level benchmark of DSVFET and FinFET was conducted on a 32bit RISC-V core, following the standard flow of synthesis, place & route and timing/power signoff. At the block level (Figs. 11(b-c)), 1NS clearly outperforms the FinFET with 17.4% lower energy per operation (or 1/EE) for 1xNS-PV at the same area, fully revealing its suitability in EEC. Besides, the chip area of 1xNS-PV is 39.6% smaller than FinFET at the same utilization and 32.5% for minimum area achieved, as validated by the layout comparison in Figs. 12(a-b). As for the EE, 1xNS-PV clearly outperforms FinFET in the full V_{DD} from 0.3 to 0.5 V in the typical EEC operation voltage range, with 15% EDP benefit @ iso-frequency (Figs. 12(c-d)).

Conclusion: In this work, a novel symmetric dual-sided VFET was proposed and experimentally demonstrated for the first time, showing ultra-scaled device geometry and nearly symmetric characteristics by simulation. From circuits and block-level study, DSVFET, especially the 1NS design, shows higher energy efficiency with smaller block area than FinFET at low V_{DD}, proving its superiority in EEC.

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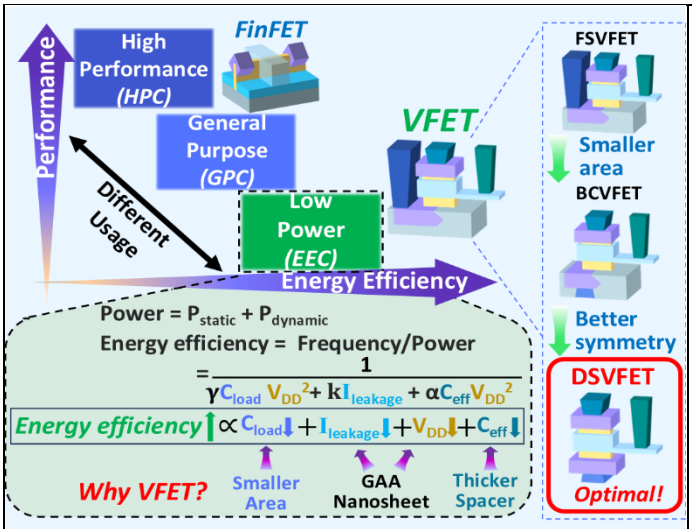

Fig. 1. Different computation paradigms of advanced logic. VFET exceeds FinFET for smaller leakage, capacitance and area with adjustable device geometry, making it better for EEC. DSVFET is proposed with best device geometry and smallest footprint.

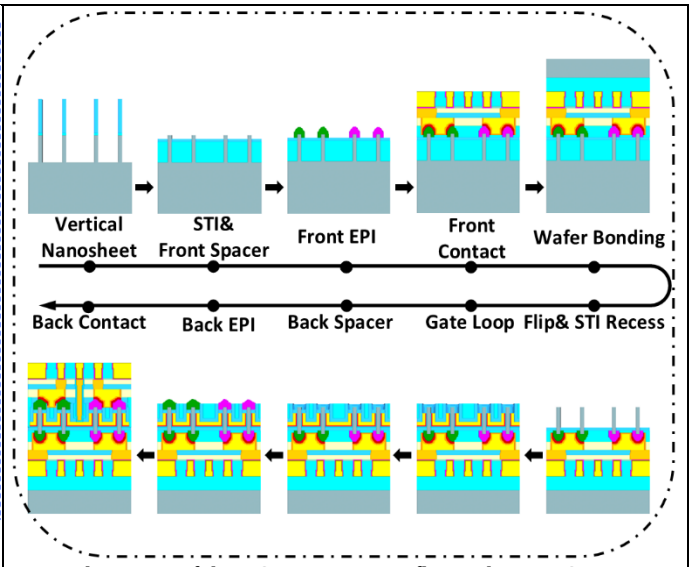

Fig. 2. key steps of the DSVFET process flow, taking 2NS INV as an example. The back S/D is formed after wafer bonding and flipping, resulting in symmetric device geometry.

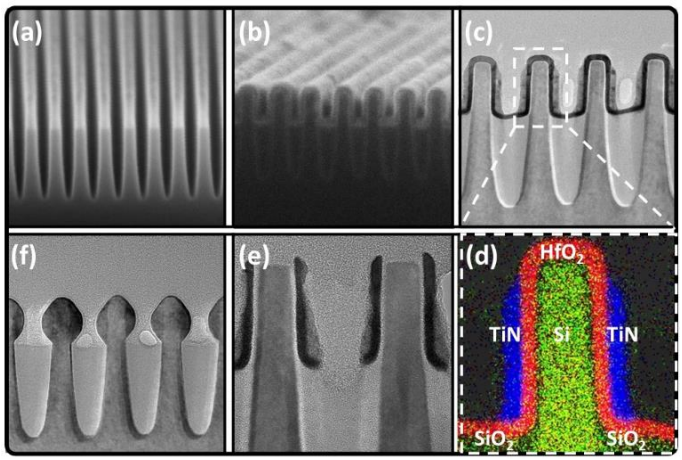

Fig. 3. Critical modules of DSVFET. (a) high aspect ratio vertical NS etching at small pitches. (b) gate stack formation with HfO_2 and TiN. (c-d) highly selective gate TiN recess and the EDS mapping. (e) gate dielectric recess. (f) selective S/D epi growth on vertical NS. All the short loops are compatible with the standard CMOS processes.

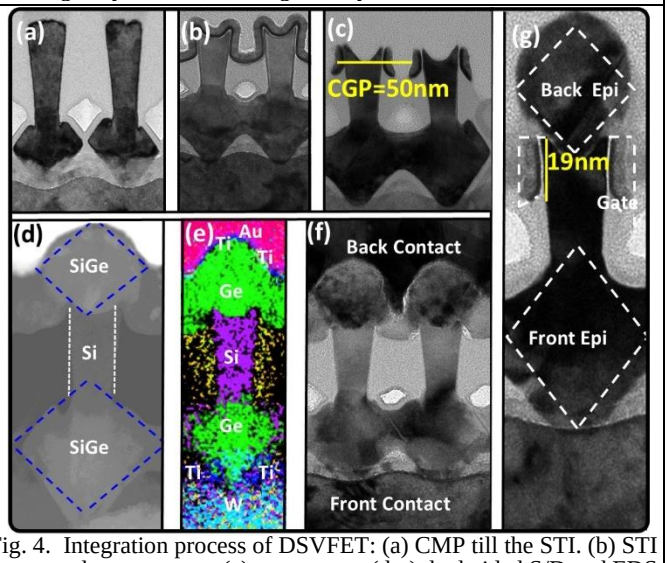

Fig. 4. Integration process of DSVFET: (a) CMP till the STI. (b) STI recess and gate process. (c) gate recess. (d-e) dual-sided S/D and EDS results. (f) dual-sided S/D and contacts with 50 nm CGP. (g) full device structure of DSVFET with 19 nm metal gate.

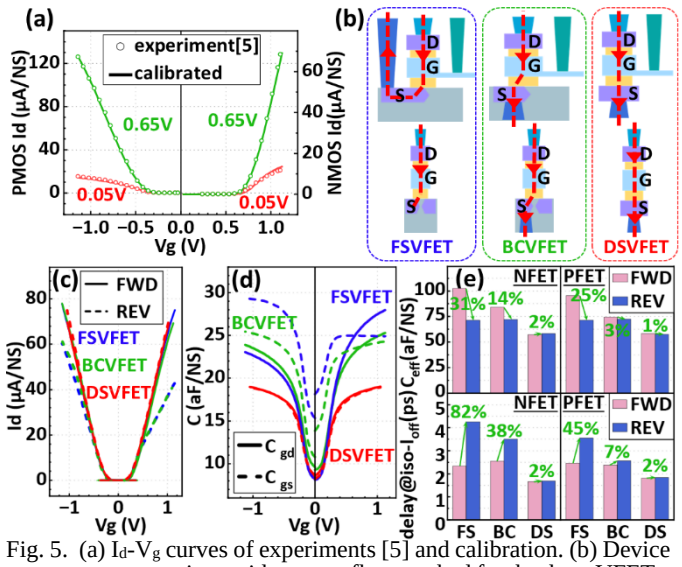

Fig. 5. (a) I_d-V_g curves of experiments [5] and calibration. (b) Device structure cross sections with current flow marked for the three VFETs. (c-d) Simulated I_dV_g and CV curves of the three. (e) C_{eff} and delay of forward and reverse modes, indicating best symmetry of DSVFET.

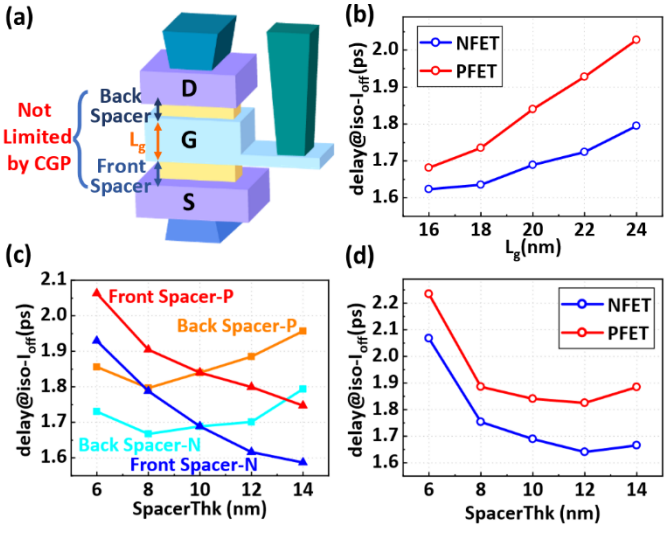

Fig. 6. (a) Important knobs at DSVFET structure level. Effects in delay@iso-I_{off} are by changing the: (b) gate length, (c) front or back spacer thickness, respectively (d) front and back spacer thickness simultaneously. Trade-off can be seen between these parameters.

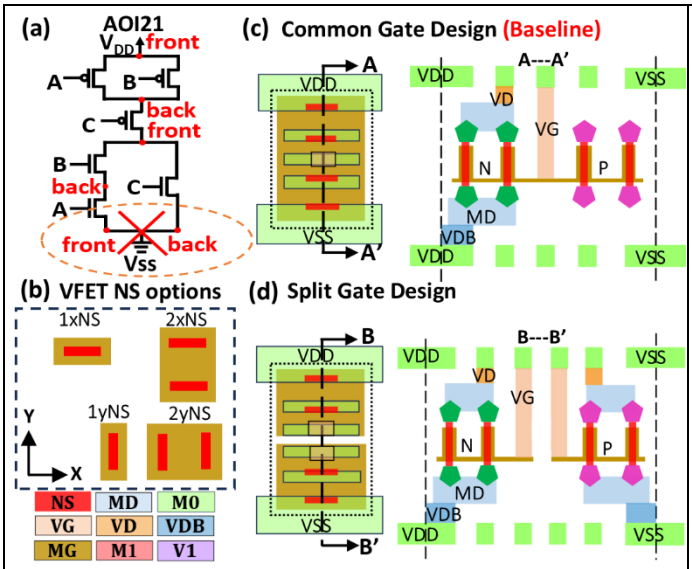

Fig. 7. (a) Dual-sided power topology, taking AOI21 as an example. (b) DSVFET's NS design options. (c-d) Layouts and cross sections of CG and SG design. CG design is the baseline due to area benefits.

TABLE I. 2NS DSVFET and FinFET design rules.

Parameter (nm)		2xNS	2yNS	FinFET
Fin Pitch		36	36	26
CH	SG	182	143	130
	CG	156	117	
M0 CD		14	12	12
M0 Pitch		28	22	22
M1 Pitch		28	24	24
L_g		20	20	16
Fspacer Thk		10	10	-
Bspacer Thk		10	10	-
CGP		36	36	48
NS Length		26	26	-
NS/Fin CD		6	6	6
W_{eff}		128 (2NS)	128 (2NS)	116 (1Fin)

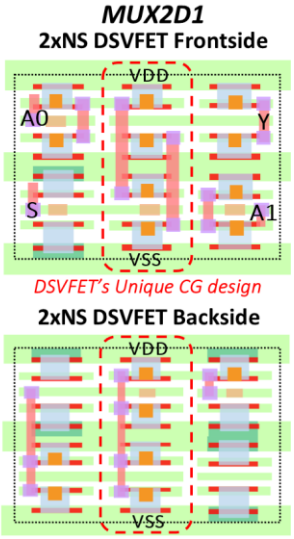

Fig. 8. MUX2D1 layouts with 2-row design for 2xNS-CG. By abutting transistors with the same input signal, as highlighted, new logic cells in VFET can be achieved with CG design without wasting area.

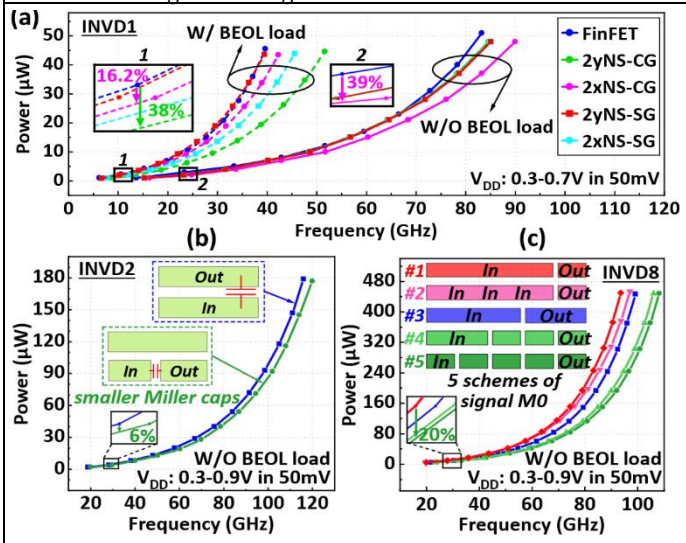

Fig. 9. (a) Power vs. frequency of different 2NS DSVFETs and FinFET. DSVFET performs better considering BEOL load. (b-c) Layout design knobs by adjusting pin positions and shapes to improve the power performance.

TABLE II. 1NS-CG DSVFET design rules.

Parameter (nm)	1yNS	1xNS	1xNS-PV
Fin Pitch	36	36	36
CH	117	104	104
M0 CD	12	12	14
M0 pitch	22	22	28
M1 Pitch	24	28	28
L_g	20	20	20
Fspacer Thk	10	10	10
Bspacer Thk	10	10	10
NS Length	26	26	26
W_{eff}	64 (1NS)	64 (1NS)	64 (1NS)

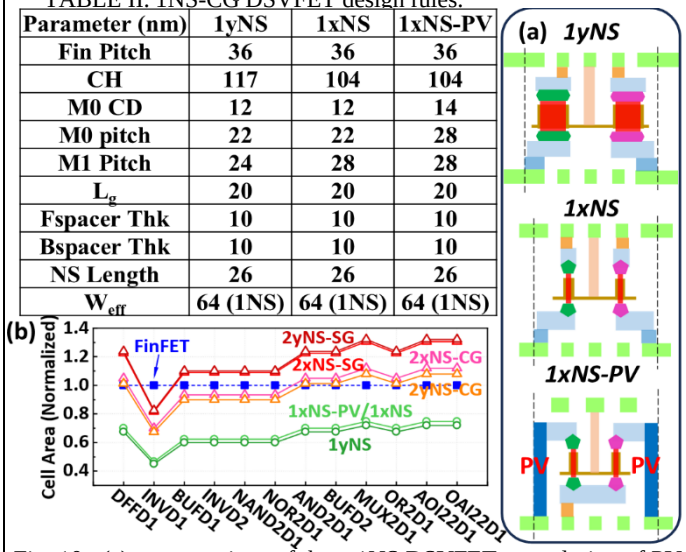

Fig. 10. (a) cross sections of three 1NS DSVFET, new design of PV is introduced. (b) standard cell areas comparison between DSVFET and FinFET. All 1NS cells are smaller than FinFET.

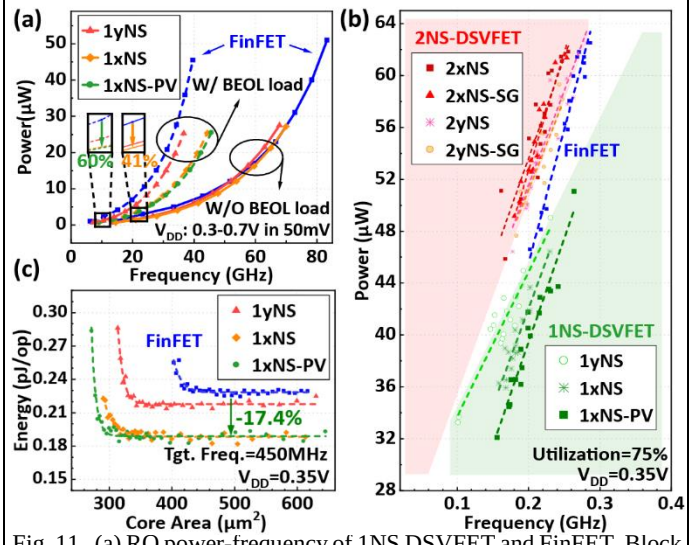

Fig. 11. (a) RO power-frequency of 1NS DSVFET and FinFET. Block level benchmarks based on 32-bit RISC-V core designed for DSVFET and FinFET: (b) Power-frequency and (c) Energy-Area relations. 1NS has clearly lower energy than FinFET.

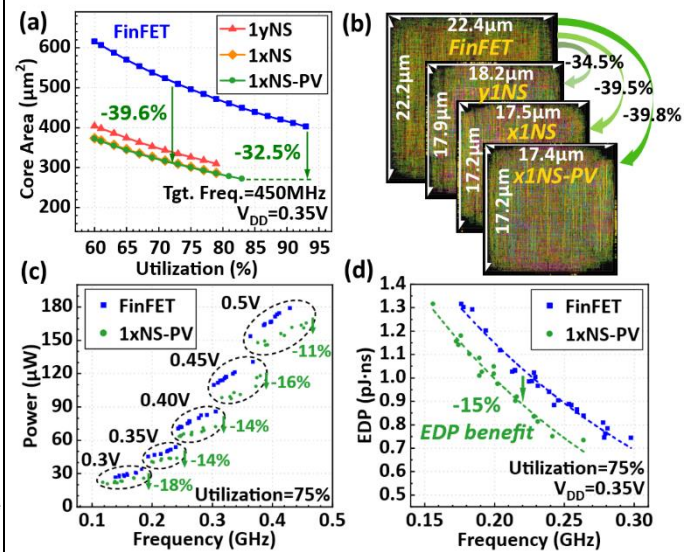

Fig. 12. Block level readouts on 1NS DSVFET and FinFET: (a) Area benefits by 1NS DSVFET, as further validated by the core layout (b). (c) 1xNS-PV exceeds FinFET at various V_{DD}, (d) EDP vs. frequency.